

[illegible]

Fig. 3

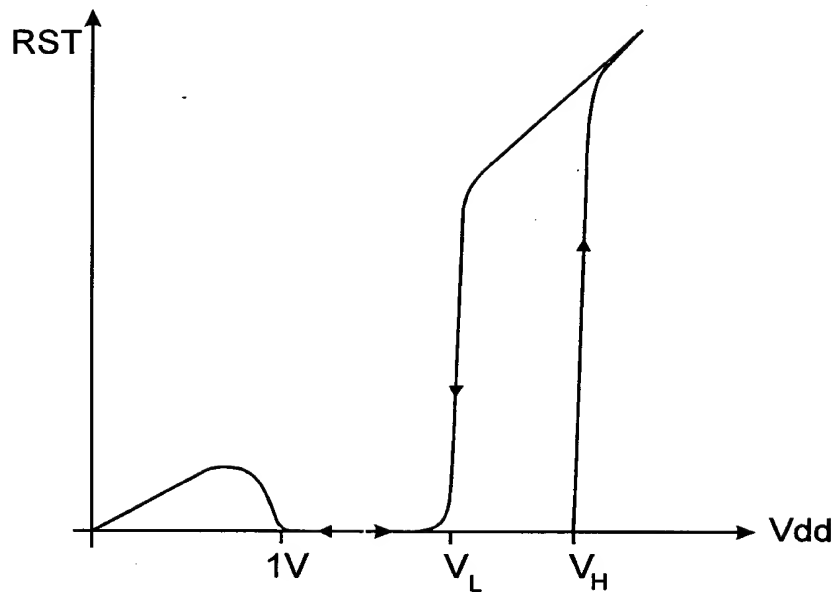


Fig . 4

MICROPROCESSOR		ANTENNA INTERFACE	
CONTACT MODE	CONTACTLESS MODE	CONTACT MODE	CONTACTLESS MODE
Vdd = RST = CLK = IO ₂ = 0 ⇒ C.M DATA via IO ₁ C.M { data trans- action ISO 7816	Vdd = RST = CLK = IO ₂ = 1 ⇒ C / L DATA via IO ₂ C/L { data trans- action CONTACTLESS PROTOCOL	Vdd = RST, CLK = TRISTATE E / M FIELD OFF ⇒ C.M. MODE	Vdd = RST = CLK = E / M FIELD ON ⇒ C/L. MODE DATA TRANS- ACTION via IO ₂

Fig . 5

00001340-123097
/60E2T" 042T0060

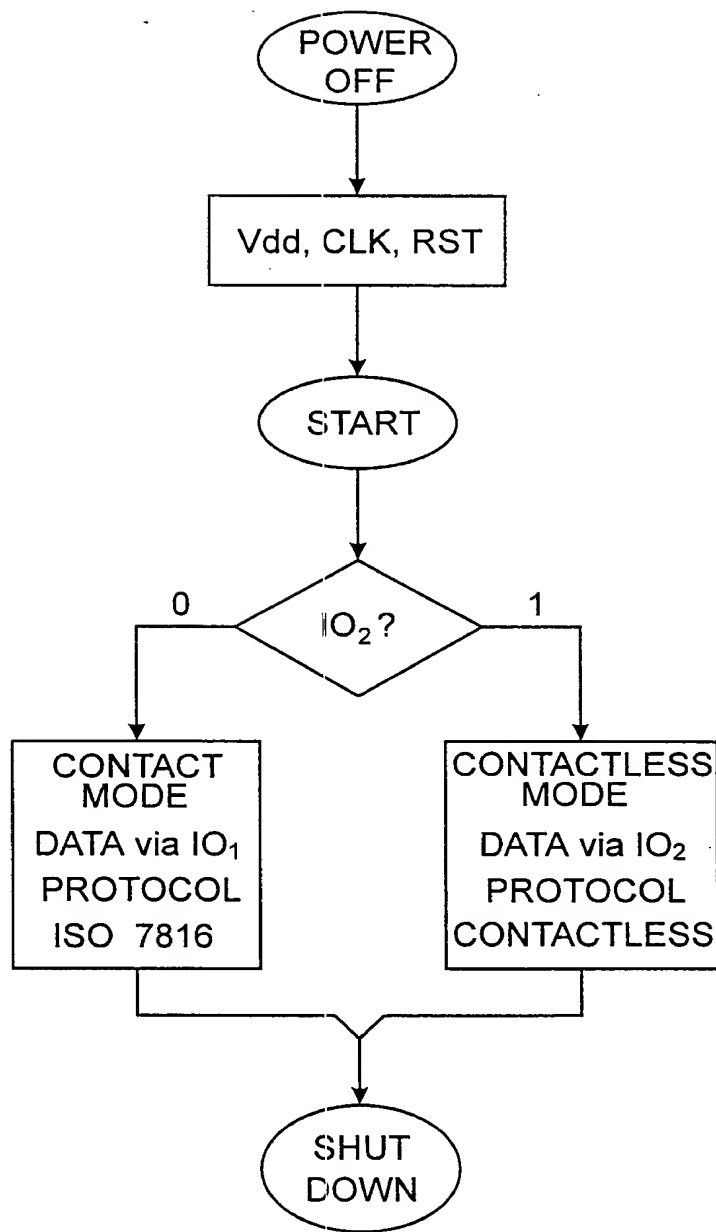


Fig. 6

09001240 123057

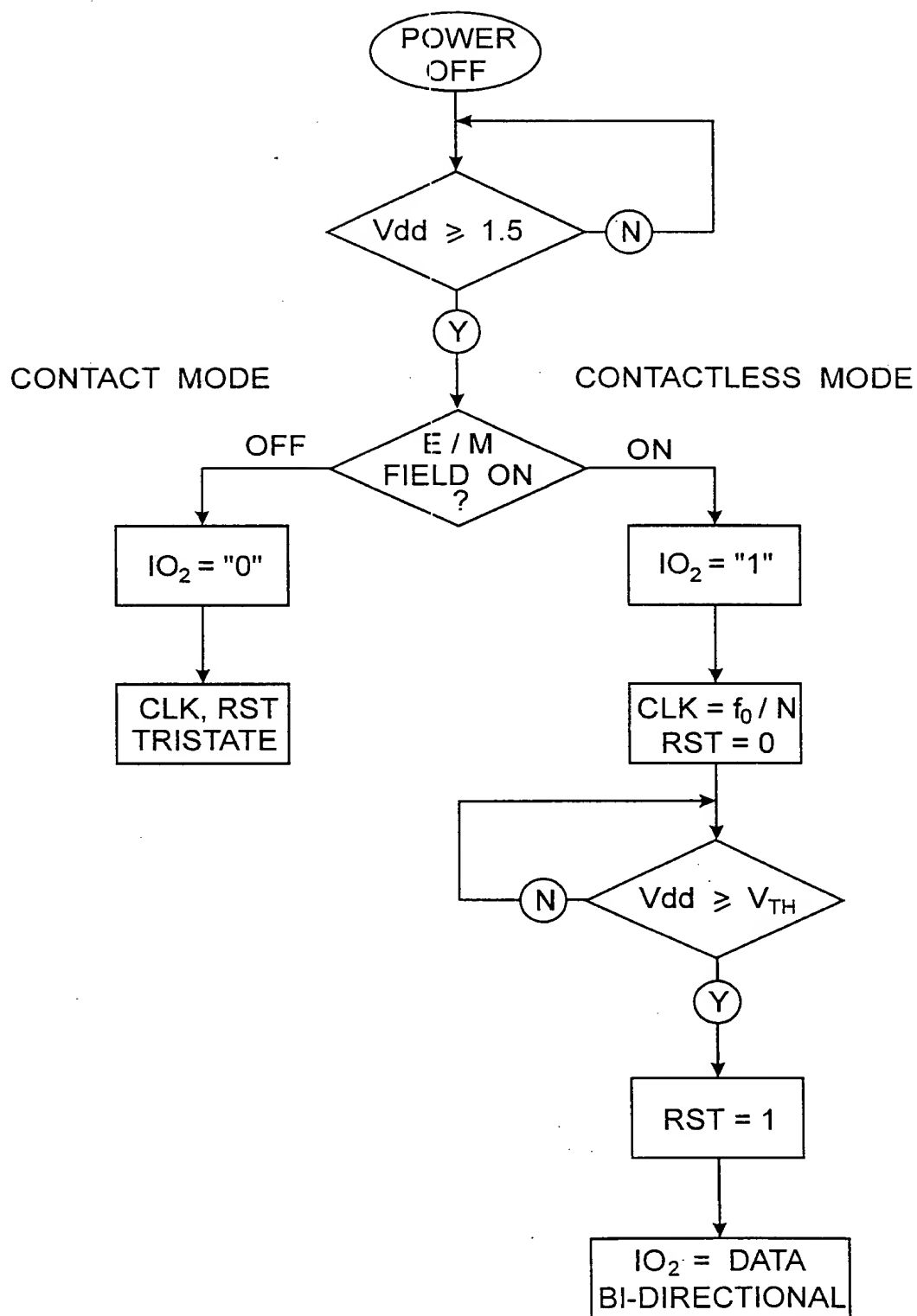


Fig. 7

0000140-12307
SECRET

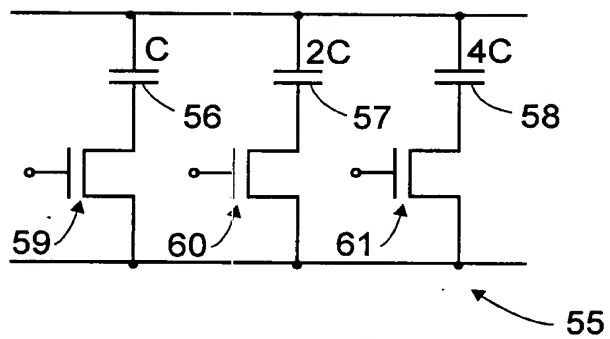


Fig. 8 a

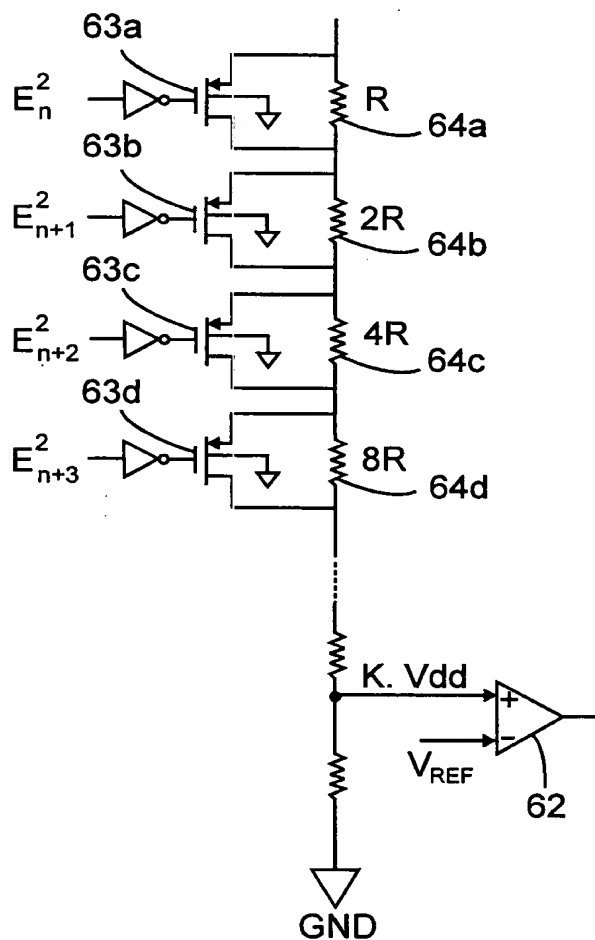


Fig. 8 b

The diagram illustrates a microprocessor system (10) with an antenna interface (15). The system includes a microprocessor (14) with pins Vdd, IO₁, IO₂, RST, CLK, and GND. The antenna interface (15) contains a coil (20, 21) connected to pins 15 and 21. The interface also includes a reference voltage (V_{ref}) and a bridge circuit (37) connected to the microprocessor's IO₁ pin. The bridge circuit (37) is connected to a clamp circuit (39) and a variable capacitor (E², 38). The system also features a data communications circuit (65) connected to the microprocessor's IO₂ pin. The data communications circuit (65) includes a data input/output (DATA i/o) block, a data input (DATIN), a data output (DATOUT), and a data input/output (DATA i/o) block. The data communications circuit (65) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a contact mode detector (52) connected to the microprocessor's RST pin. The contact mode detector (52) is connected to a coil (20) and a variable capacitor (E², 38). The system also includes an EEPROM (53) connected to the microprocessor's CLK pin. The EEPROM (53) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a clock circuit (51) connected to the microprocessor's CLK pin. The clock circuit (51) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a reset circuit (50) connected to the microprocessor's RST pin. The reset circuit (50) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a programming unit (54) connected to the microprocessor's CLK pin. The programming unit (54) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a pulse output (PULOUT) and a pulse input (PULIN) connected to the microprocessor's GND pin. The pulse output (PULOUT) and pulse input (PULIN) are connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a contact mode detector (52) connected to the microprocessor's RST pin. The contact mode detector (52) is connected to a coil (20) and a variable capacitor (E², 38). The system also includes an EEPROM (53) connected to the microprocessor's CLK pin. The EEPROM (53) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a clock circuit (51) connected to the microprocessor's CLK pin. The clock circuit (51) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a reset circuit (50) connected to the microprocessor's RST pin. The reset circuit (50) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a programming unit (54) connected to the microprocessor's CLK pin. The programming unit (54) is connected to a coil (20, 21) and a variable capacitor (E², 38). The system also includes a pulse output (PULOUT) and a pulse input (PULIN) connected to the microprocessor's GND pin. The pulse output (PULOUT) and pulse input (PULIN) are connected to a coil (20, 21) and a variable capacitor (E², 38).

Fig. 9

Fig. 10

Fig. 11

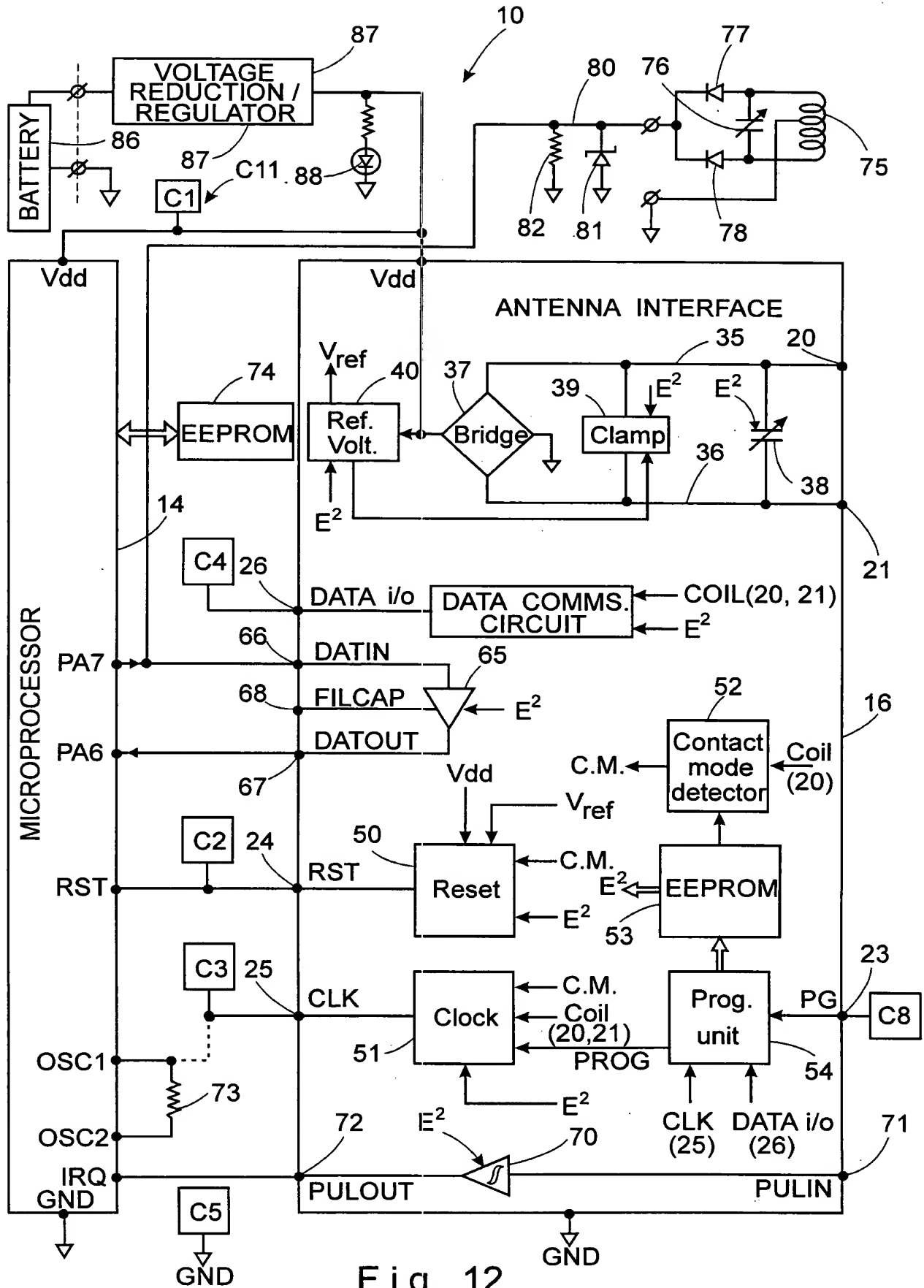


Fig. 12